

M.KUMARASAMY COLLEGE OF ENGINEERING, KARUR
(Autonomous)

CURRICULUM I TO IV SEMESTERS

ELECTRONICS AND COMMUNICATION ENGINEERING

M.E – VLSI DESIGN

REGULATION – 2013

With effect from the academic year 2013-2014

SEMESTER – I

Course Code	Course Title	Hours /Week			Credit	Maximum Marks		
		L	T	P		CIA	ESE	Total
THEORY								
PMA13104	Applied Mathematics for Electronics Engineers	3	1	0	4	50	50	100
PVL13101	DSP Integrated Circuits	3	0	0	3	50	50	100
PVL13102	Advanced Digital System Design	3	1	0	3	50	50	100
PVL13103	VLSI Design Techniques	3	1	0	3	50	50	100
PVL13104	Solid State Device Modeling and Simulation	3	0	0	3	50	50	100
E1	Elective I	3	0	0	3	50	50	100
PRACTICAL								
PVL13105P	VLSI Design Lab I	0	0	4	2	50	50	100
Total					21	700		

SEMESTER – II

Course Code	Course Title	Hours /Week			Credit	Maximum Marks		
		L	T	P		CIA	ESE	Total
THEORY								
PVL13201	Analysis and Design of Analog Integrated Circuits	3	0	0	3	50	50	100
PVL13202	CAD for VLSI Circuits	3	1	0	3	50	50	100
PVL13203	Computer Architecture and Parallel Processing	2	0	2	3	50	50	100
PVL13204	Embedded Systems	3	0	0	3	50	50	100
E2	Elective II	3	0	0	3	50	50	100
E3	Elective III	3	0	0	3	50	50	100
PRACTICAL								
PVL13205 P	VLSI Design Lab II	0	0	4	2	50	50	100
Total					20	700		

SEMESTER- III

Course Code	Course Title	Hours/Week			Credit	Maximum Marks		
		L	T	P		CIA	ESE	Total
THEORY								
E4	Elective IV	3	0	0	3	50	50	100
E5	Elective V	3	0	0	3	50	50	100
E6	Elective VI	3	0	0	3	50	50	100
PRACTICAL								
PVL13301P	Project Work Phase I	0	0	12	6	100	100	200
Total					15	500		

SEMESTER – IV

Course Code	Course Title	Hours /Week			Credit	Maximum Marks		
		L	T	P		CIA	ESE	Total
PRACTICAL								
PVL13401P	Project Work Phase II	0	0	24	12	200	200	400
Total					12	400		

LIST OF ELECTIVES

S.No	Course Title	Hours /Week			Credit	Maximum Marks		
		L	T	P		CIA	ESE	Total
SEMESTER I- ELECTIVE I								
PVL13151	Analog VLSI Design	3	0	0	3	50	50	100
PVL13152	Introduction to MEMS System Design	3	0	0	3	50	50	100
PVL13153	VLSI Technology	3	0	0	3	50	50	100
SEMESTER II- ELECTIVE II & III								
PVL13251	Genetic Algorithms and their Applications	3	0	0	3	50	50	100
PVL13252	Low Power VLSI Design	3	0	0	3	50	50	100
PVL13253	Neural Networks, Architectures and Applications	3	0	0	3	50	50	100
PVL13254	ASIC Design	3	0	0	3	50	50	100
PVL13255	Mixed Signal IC design	3	0	0	3	50	50	100
PVL13256	Physical Design of VLSI Circuits	3	0	0	3	50	50	100
SEMESTER III- ELECTIVE IV , V & VI								
PVL13350	Advanced Microprocessors and Microcontrollers	3	0	0	3	50	50	100
PVL13351	CMOS VLSI Design	3	0	0	3	50	50	100
PVL13352	Reliability Engineering	3	0	0	3	50	50	100
PVL13353	VLSI Signal Processing	3	0	0	3	50	50	100
PVL13354	Design of Semiconductor Memories	3	0	0	3	50	50	100
PVL13355	Digital Speech Signal Processing	3	0	0	3	50	50	100
PVL13356	Electromagnetic Interference and Compatibility in System Design	3	0	0	3	50	50	100
PVL13357	Wireless Embedded Systems	3	0	0	3	50	50	100

PVL13358	DSP Processor Architecture and programming	3	0	0	3	50	50	100
PVL13359	Optimization Techniques and their Applications in VLSI Design	3	0	0	3	50	50	100
PVL133510	System On Chip Design	3	0	0	3	50	50	100
PVL133511	Testing of VLSI Circuits	3	0	0	3	50	50	100

UNIT I FUZZY LOGIC**9**

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II MATRIX THEORY**9**

Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition – Toeplitz matrices and some applications.

UNIT III ONE DIMENSIONAL RANDOM VARIABLES**9**

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT IV DYNAMIC PROGRAMMING**9**

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V QUEUEING MODELS**9**

Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula - Machine Interference Model – Steady State analysis – Self Service queue.

L = 45: T=15; Total: 45 Hours**REFERENCES:**

1. George J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt. Ltd., 1997.
2. Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing, Pearson Education, 2000.
3. Richard Johnson, Miller & Freund's Probability and Statistics for Engineers, 7th Edition, Prentice – Hall of India, Private Ltd., New Delhi (2007).
4. Taha, H.A., Operations Research, An introduction, 7th edition, Pearson education editions, Asia, New Delhi, 2002.
5. Donald Gross and Carl M. Harris, Fundamentals of Queueing theory, 2nd edition, John Wiley and Sons, New York (1985).

UNIT I DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES 9

Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

UNIT II DIGITAL SIGNAL PROCESSING 9

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

UNIT III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT IV DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES 9

DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

UNIT V ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN 9

Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies. Cordic algorithm.

TOTAL: 45**REFERENCES:**

1. Lars Wanhammer, "DSP Integrated Circuits", 1999 Academic press, New York.
2. A.V.Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2000.
3. Emmanuel C. Ifeakor, Barrie W. Jervis, "Digital signal processing – A practical approach", Second Edition, Pearson Education, Asia.
4. Keshab K.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.
5. Givone Donald G., "Digital Principles and Design", Tata McGraw-Hill, New Delhi, 2002.

UNIT I SEQUENTIAL CIRCUIT DESIGN**9**

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits-design of iterative circuits-ASM chart and realization using ASM.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN**9**

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS**9**

Fault table method-path sensitization method – Boolean difference method-D algorithm -Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES**9**

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000.

UNIT V SYSTEM DESIGN USING VHDL**9**

VHDL operators – Arrays – concurrent and sequential statements – packages- Data flow – Behavioral – structural modeling – compilation and simulation of VHDL code –Test bench - Realization of combinational and sequential circuits using HDL – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

TOTAL: 45**REFERENCES:**

1. Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004.
- 2 .Nripendra N Biswas “Logic Design Theory” Prentice Hall of India, 2001.
3. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications, 2002.
4. Parag K.Lala “Digital system Design using PLD” B S Publications, 2003.
5. Charles H Roth Jr.”Digital System Design using VHDL” Thomson learning, 2004.
6. Douglas L.Perry “VHDL programming by Example” Tata McGraw. Hill – 2006.

UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY 9

NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.

UNIT II INVERTERS AND LOGIC GATES 9

NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION 9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN 9

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modeling, cross talk, floor planning, power distribution. Clock distribution. Basics of CMOS testing.

UNIT V VERILOG HARDWARE DESCRIPTION LANGUAGE 9

Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.

TOTAL: 45**REFERENCES:**

1. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
2. John P.Uyemura "Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc., 2002.
3. Samir Palnitkar, "Verilog HDL", Pearson Education, 2nd Edition, 2004.
4. Eugene D.Fabricius, Introduction to VLSI Design McGraw Hill International Editions, 1990.
5. J.Bhasker, B.S.Publications, "A Verilog HDL Primer", 2nd Edition, 2001.
6. Pucknell, "Basic VLSI Design", Prentice Hall of India Publication, 1995.
7. Wayne Wolf "Modern VLSI Design System on chip. Pearson Education. 2002.

UNIT I MOSFET DEVICE PHYSICS	9
MOSFET capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.	
UNIT II NOISE MODELING	9
Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuits	
UNIT III BSIM4 MOSFET MODELING	9
Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, noise model, junction diode models, Layout-dependent parasitics model.	
UNIT IV OTHER MOSFET MODELS	9
The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Nonquasi- static modeling, noise model temperature effects, MOS model 9, MOSAI model)	
UNIT V MODELLING OF PROCESS VARIATION AND QUALITY ASSURANCE	9
Influence of process variation, modeling of device mismatch for Analog/RF Applications, Benchmark circuits for quality assurance, Automation of the tests	

TOTAL: 45

REFERENCES:

1. Trond Ytterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd.

1. Modeling of Sequential Digital system using VHDL.
2. Modeling of Sequential Digital system using Verilog.
3. Design and Implementation of ALU using FPGA.
4. Simulation of NMOS and CMOS circuits using SPICE.
5. Modeling of MOSFET using System C.
6. Implementation of FFT, Digital Filters in DSP Processor.
7. Implementation of DSP algorithms using Software Package
8. Implementation of MAC Unit using FPGA.

UNIT I MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES 9

Depletion region of a PN junction – large signal behavior of bipolar transistors small signal model of bipolar transistor- large signal behavior of MOSFET- small signal model of the MOS transistors- short channel effects in MOS transistors – weak inversion in MOS transistors- substrate current flow in MOS transistor.

UNIT II CIRCUIT CONFIGURATION FOR LINEAR IC 9

Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references. Output stages: Emitter follower, source follower and Push pull output stages.

UNIT III OPERATIONAL AMPLIFIERS 9

Analysis of operational amplifiers circuit, slew rate model and high frequency analysis, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise

UNIT IV ANALOG MULTIPLIER AND PLL 9

Analysis of four quadrant and variable trans conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY 9

MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic-Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers

TOTAL: 45 Hours

REFERENCES:

1. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog IC's", Fourth Edition, Willey International, 2002.
2. Behzad Razavi, "Principles of data conversion system design", S.Chand and company ltd, 2000.
3. Nandita Dasgupata, Amitava Dasgupta,"Semiconductor Devices, Modeling and Technology", Prentice Hall of India pvt. ltd, 2004.
4. Grebene, Bipolar and MOS Analog Integrated circuit design", John Wiley & sons, Inc., 2003.
5. Phillip E.Allen Douglas R. Holberg, "CMOS Analog Circuit Design", Second Edition-Oxford University Press-2003

UNIT I VLSI DESIGN METHODOLOGIES**9**

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems – general purpose methods for combinatorial optimization.

UNIT II DESIGN RULES**9**

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation – Placement algorithms - partitioning

UNIT III FLOOR PLANNING**9**

Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION**9**

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams – Two Level Logic Synthesis.

UNIT V MODELLING AND SYNTHESIS**9**

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm – Assignment problem - High level transformations.

TOTAL: 45 Hours**REFERENCES:**

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

UNIT I THEORY OF PARALLELISM**9**

Parallel computer models - the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties- Conditions of parallelism.

UNIT II PARTITIONING AND SCHEDULING**9**

Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures. Principles of scalable performance – performance matrices and measures, parallel processing applications, speedup performance laws, scalability analysis and approaches.

UNIT III HARDWARE TECHNOLOGIES**9**

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory - backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.

UNIT IV PIPELINING AND SUPERSCALAR TECHNOLOGIES**9**

Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V SOFTWARE AND PARALLEL PROGRAMMING**9**

Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TOTAL: 45**REFERENCES:**

1. Kai Hwang, " Advanced Computer Architecture ", McGraw Hill International, 2001.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer architecture – A design Space Approach", Pearson Education, 2003.
3. John P. Shen, "Modern processor design . Fundamentals of super scalar processors", Tata McGraw Hill 2003.
4. Kai Hwang, "Scalable parallel computing", Tata McGraw Hill 1998.
5. William Stallings, " Computer Organization and Architecture", Macmillan Publishing Company, 1990.
6. M.J. Quinn, " Designing Efficient Algorithms for Parallel Computers", McGraw Hill International, 1994.
7. Barry, Wilkinson, Michael, Allen "Parallel Programming", Pearson Education Asia , 2002.
8. Harry F. Jordan Gita Alaghband, " Fundamentals of parallel Processing", Pearson Education , 2003.
9. Richard Y.Kain, " Advanced computer architecture –A systems Design Approach", PHI, 2003.

UNIT I EMBEDDED PROCESSORS**9**

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioural Description, Embedded systems on a chip (SOC) and the use of VLSI designed circuits Design Example: Model Train Controller, ARM processor- processor and memory organization.

UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM**9**

Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock, Hybrid Architecture.

UNIT III NETWORKS**9**

Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, USB, CAN Bus, Advanced serial high speed buses, SHARC link supports, Ethernet, Martinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

UNIT IV REAL TIME OPERATING SYSTEMS**9**

Tasks and Task States, Tasks and Data, Semaphores and Shared Data, Message Queues, Mailboxes and Pipes, Timer functions, Events, Memory Management, Interrupt Routines in RTOS Environment, Case Study of Programming with RTOS.

UNIT V SYSTEM DESIGN TECHNIQUES**9**

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

TOTAL: 45**REFERENCES:**

1. Wayne Wolf, "Computers as Components - Principles of Embedded Computing System Design", Morgan Kaufman Publishers, First Indian Reprint, 2001.
2. Jane.W.S. Liu, "Real-Time systems", Pearson Education Asia.
3. Rajkamal, "Embedded Systems Architecture, Programming and Design", TMH, First reprint, 2003.
4. C. M. Krishna and K. G. Shin, "Real-Time Systems", McGraw-Hill, 1997
5. Frank Vahid and Tony Givargis, "Embedded System Design: A Unified Hardware/Software Introduction", John Wiley & Sons.

- 1.) Implementation of 8 Bit ALU in FPGA / CPLD.
- 2.) Implementation of 4 Bit Sliced processor in FPGA / CPLD.
- 3.) Implementation of Elevator controller using embedded microcontroller.
- 4.) Implementation of Alarm clock controller using embedded microcontroller.
- 5.) Implementation of model train controller using embedded microcontroller.
- 6.) System design using PLL.

UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW- VOLTAGE SIGNAL PROCESSING 9

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOSTransistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS,Bipolar and Low-Voltage BiCMOS Op- Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING 9

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models- Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS 9

First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched- Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters- Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma- Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filtersmechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS 9

Fault modelling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses- Design for Electron - Beam Testability-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTERAIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT 9

Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation- Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout- Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

TOTAL: 45

REFERENCES:

1. Mohammed Ismail, Terri Fiez, "Analog VLSI signal and Information Processing ", McGraw-Hill International Editons, 1994.
2. Malcom R.Haskard, Lan C.May, "Analog VLSI Design - NMOS and CMOS ", Prentice Hall, 1998.
3. Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990.
4. Jose E.France, Yannis Tsvividis, "Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994.

UNIT I INTRODUCTION TO MEMS 9

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Microaccelerometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II MECHANICS FOR MEMS DESIGN 9

Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III ELECTRO STATIC DESIGN 9

Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.

UNIT IV CIRCUIT AND SYSTEM ISSUES 9

Electronic Interfaces, Feedback systems, Noise, Circuit and system issues, Case studies – Capacitive accelerometer, Piezo electric pressure sensor, Modelling of MEMS systems, CAD for MEMS.

UNIT V INTRODUCTION TO OPTICAL AND RF MEMS 9

Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues.

TOTAL: 45**REFERENCES:**

1. Stephen Santuria, " Microsystems Design", Kluwer publishers, 2000.
2. Nadim Maluf, " An introduction to Micro electro mechanical system design", Artech House, 2000.
3. Mohamed Gad-el-Hak, editor, " The MEMS Handbook", CRC press Boca Raton, 2000.
4. Tai Ran Hsu, " MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.

UNIT I CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION 9

Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II LITHOGRAPHY AND RELATIVE PLASMA ETCHING 9

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments.

UNIT III DEPOSITION, DIFFUSION, ION IMPLEMENTATION AND METALISATION 9

Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism – Measurement techniques - Range theory- Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapour deposition – Patterning.

UNIT IV PROCESS SIMULATION AND VLSI PROCESS INTEGRATION 9

Ion implantation – Diffusion and oxidation – Epitaxy – Lithography – Etching and Deposition- NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology - Bipolar IC Technology – IC Fabrication.

UNIT V ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES 9

Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – banking design consideration – VLSI assembly technology – Package fabrication technology.

TOTAL: 45**REFERENCES:**

1. S.M.Sze, "VLSI Technology", Mc.Graw.Hill Second Edition. 2002.
2. Douglas A. Pucknell and Kamran Eshraghian, " Basic VLSI Design", Prentice Hall India. 2003.
3. Amar Mukherjee, "Introduction to NMOS and CMOS VLSI System design Prentice Hall India.2000.
4. Wayne Wolf , "Modern VLSI Design", Prentice Hall India.1998.

UNIT I **9**

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion

UNIT II **9**

GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy- Multiway Partitioning

UNIT III **9**

Hybrid genetic – genetic encoding-local improvement-WDFR-Comparison of Cas- Standard cell placement-GASP algorithm-unified algorithm.

UNIT IV **9**

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures.

UNIT V **9**

Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.

TOTAL: 45

REFERENCES:

1. Pinaki Mazumder,E.MRudnick,"Genetic Algorithm for VLSI Design,Layout and test Automation", Prentice Hall,1998.
2. Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" Wiley – Interscience,1977.
3. Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms", CRC press, 1st Edition Dec 2001.
4. John R.Koza, Forrest H.Bennett III, David Andre , Morgan Kufmann, "Genetic Programming Automatic programming and Automatic Circuit Synthesis", 1st Edition , May 1999.

UNIT I POWER DISSIPATION IN CMOS 9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.

UNIT II POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION 9

Power Estimation technique – logic power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9

Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45**REFERENCES:**

1. Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, 2000.
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power", Kluwer, 2002.
3. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999.
4. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995.
5. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.
6. Abdelatif Belaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, 1995.
7. James B.Kulo, Shih-Chia Lin, "Low voltage SOI CMOS VLSI devices and Circuits", John Wiley and sons, inc. 2001.

UNIT I BACK PROPAGATION**10**

Introduction to Artificial Neural Systems - Perceptrons - Representation - Linear separability - Learning – Training algorithm - The back propagation network - The generalized delta rule - Practical considerations – BPN applications - traveling sales man problem.

UNIT II STATISTICAL METHODS**10**

Hopfield nets - Cauchy training - Simulated annealing - The Boltzmann machine. Associative memory - Bidirectional associative memory - Applications.

UNIT III COUNTER PROPAGATION NETWORK AND SELF ORGANIZING MAPS**10**

CPN building blocks - CPN data processing. SOM data processing - Applications.

UNIT IV ADAPTIVE RESONANCE THEORY AND SPATIO TEMPORAL PATTERN CLASSIFICATION**10**

ART network description - ART1-ART2 - Application. The formal avalanche - Architecture of spatio temporal networks - The sequential competitive avalanche field - Applications of STNs.

UNIT V NEO – CONGNITRON**10**

Cognitron - Structure & training - The neocognitron architecture - Data processing – Performance - Addition of lateral inhibition and feedback to the neocognitron. Optical neural networks - Holographic correlators.

TOTAL: 50**REFERENCES:**

1. James Freeman A. and David Skapura M., Neural Networks - Algorithms, Applications & Programming Techniques Addison Wesley, 1992.
2. Yegnanarayana B., Artificial Neural Networks, Prentice Hall of India Private Ltd., NewDelhi, 1999.
3. Laurence Fausett, “Fundamentals of Neural Networks: Architecture, Algorithms and Applications”, Prentice Hall, 1994.
4. Simon Haykin, “Neural Networks: A Comprehensive Foundation”, 2nd Edition, Prentice Hall India, 2002.

UNIT I INTRODUCTION TO ASICs, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors – Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

UNIT II PROGRAMMABLE ASICs, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 – Altera FLEX Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 9

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL: 45**REFERENCES:**

1. M.J.S .Smith, "Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997.
2. Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.
3. Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.
4. R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House Publishers, 2000.
5. F. Nekoogar. Timing Verification of Application-Specific Integrated Circuits (ASICs). Prentice Hall PTR, 1999.

UNIT I DATA CONVERTER MODELLING 9

Sampling and aliasing, SPICE models for DAC, ADCs, Quantization noise.

UNIT II DATA CONVERTER SNR 9

Overview, Improving SNR using Averaging, Using feedback to improve SNR. Noise shaping Data Converters- Noise shaping fundamentals, Noise shaping topologies.

UNIT III SUBMICRON CMOS CIRCUIT DESIGN 9

Overview and models, Digital circuit design, Analog circuit design.

UNIT IV IMPLEMENTATION OF DATA CONVERTERS 9

R-2R Topologies for DACs, Op-Amp in Data Converters, Implementing DACs

UNIT V INTEGRATOR- BASED CMOS FILTERS 9

Building Blocks, Filtering topologies, filters using Noise- shaping, Push-pull amplifier, 1st order Noise shaping modulator, measuring 1/F noise, discrete analog integrator, quantization noise.

TOTAL: 45

REFERENCES

1. Jacob Baker.R., CMOS Mixed signal circuit design, Wesley – IEEE, 2000.
2. Allen Holberg, CMOS Analog Circuit Design, PHI
3. Baker, CMOS Circuit Design, Layout and Simulation, Wiley

UNIT I INTRODUCTION TO VLSI TECHNOLOGY**9**

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates,field programmable gate array(FPGA)-layout methodologies- Packaging-Computational Complexity- Algorithmic Paradigms.

UNIT II PLACEMENT USING TOP-DOWN APPROACH**9**

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic- Ratiocut- partition with capacity and i/o constraints. Floor planning: Rectangular dual floor planning- hierarchial approach-simulated annealing- Floor plan sizing.

Placement: Cost function- force directed method- placement by simulated annealingpartitioning placement- module placement on a resistive network – regular placementlinear placement.

UNIT III ROUTING USING TOP DOWN APPROACH**9**

Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches- hierarchial approaches- multicommodity flow based techniques- Randomised Routing- One Step approach- Integer Linear Programming.

Detailed Routing: Channel Routing- Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs.

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT**9**

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing Driving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization.

UNIT V SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION**9**

Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing- Multiple chip modules(MCM)- Programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

TOTAL: 45**REFERENCES:**

1. Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", Mc Graw Hill International Edition 1995
2. Preas M. Lorenzatti, "Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.

UNIT I MICROPROCESSOR ARCHITECTURE**9**

Instruction set – Data formats – Instruction formats – Addressing modes – Memory hierarchy – register file – Cache – Virtual memory and paging – Segmentation – Pipelining – The instruction pipeline – pipeline hazards – Instruction level parallelism – reduced instruction set – Computer principles – RISC versus CISC – RISC properties – RISC evaluation – On-chip register files versus cache evaluation.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM**9**

The software model – functional description – CPU pin descriptions – RISC concepts – bus operations – Super scalar architecture – pipe lining – Branch prediction – The instruction and caches – Floating point unit –protected mode operation – Segmentation – paging – Protection – multitasking – Exception and interrupts – Input /Output – Virtual 8086 model – Interrupt processing – Instruction types – Addressing modes – Processor flags – Instruction set –programming the Pentium processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM**9**

The ARM architecture – ARM assembly language program – ARM organization and implementation – The ARM instruction set – The thumb instruction set – ARM CPU cores.

UNIT IV MOTOROLA 68HC11 MICRO CONTROLLERS**9**

Instructions and addressing modes – operating modes – Hardware reset – Interrupt system Parallel I/O ports – Flags – Real time clock – Programmable timer – pulse accumulator – serial communication interface – A/D converter, PWM and UART – hardware expansion – Assembly language Programming.

UNIT V PIC MICRO CONTROLLER**9**

CPU architecture – Instruction set – Interrupts – Timers – I/O port expansion – I²C bus for peripheral chip access – A/D converter, UART and PWM – Introduction to C Compilers.

TOTAL: 45**REFERENCES:**

1. Daniel Tabak, "Advanced Microprocessors", McGraw Hill.Inc.,1995.
2. James L Antonakos, "The Pentium Microprocessor", Pearson Education.,1997.
3. Steve Furber, "ARM System – On Chip architecture", Addison Wesley.,2000.
4. John B Peatman, "Design with PIC Microcontroller, Prentice hall. 1997.
5. Valvano, "Embedded Microcomputer System", Thomson Asia Pvt.Ltd., First Reprint2001.
6. Gene H Miller, "Micro Computer Engineering", Pearson Education.,2003.
7. James L Antonakos., "An Introduction to the Intel family of Microprocessors", Pearson Education.,1999.
8. Barry B Breg, "The Intel Microprocessors Architecture, Programming and Interfacing", Prentice Hall of India.,2002.

UNIT I MOS TRANSISTOR THEORY**10**

Introduction to I.C Technology. Basic MOS transistors. Threshold Voltage. Body effect. Basic D.C. Equations. Second order effects. MOS models. Small signal A.C characteristics. The complementary CMOS inverter. DC characteristics. Static Load MOS inverters. The differential inverters. Transmission gate.

UNIT II CMOS PROCESSING TECHNOLOGY.**10**

Silicon semiconductor technology. Wafer processing, Oxidation, epitaxy, deposition, Ion implantation. CMOS technology. N-well, p-well process. Silicon on insulator. CMOS process enhancement. Interconnect and circuit elements. Layout design rules. Latchup.

UNIT III CIRCUIT CHARACTERISTICS AND PERFORMANCE ESTIMATION**10**

Resistance estimation. Capacitance estimation. MOS capacitor characteristics. Device capacitances. Diffusion capacitance. SPICE modeling of MOS capacitance. Routing capacitance. Distributed RC effects. Inductance. Switching characteristics. Rise time. Fall time. Delay time. Empirical delay models. Gate delays. CMOS gate transistor sizing. Power dissipation. Scaling of MOS transistor dimensions.

UNIT IV CMOS CIRCUIT AND LOGIC DESIGN**10**

CMOS Logic gate design. Fan in and fan out. Typical CMOS NAND and NOR delays. Transistor sizing. CMOS logic structures. Complementary logic. BICMOS logic. Pseudo nMOS logic. Dynamic CMOS logic. Clocked CMOS logic. Pass transistor logic. CMOS domino logic. NP domino logic. Cascade voltage switch logic. Source follower pull up Logic (SFPL). Clocking strategies – I/O structures.

UNIT V CMOS SUBSYSTEM DESIGN**10**

Data path operations. Addition/subtraction. Parity generators. Comparators. Zero/one detectors. Binary Counters. ALUs. Multiplication. Array, Radix-n, Wallace Tree and Serial Multiplication. Shifters. Memory elements. RWM, Rom, Content Addressable Memory. Control: FSM, PLA Control Implementation.

TOTAL: 50**REFERENCES:**

1. Neil.H.E. Weste and Eshragian K, "Principles of CMOS VLSI Design". 2nd Edition. Addison-Wesley,2000.
2. Douglas a. Pucknell and Eshragian.E , "Basic VLSI Design" 3rd Edition, Prentice Hall of India , 2000.
3. Jacob Baker R., Harry W. Li., & David K. Boyce., "CMOS Circuit Design", 3rd Indian reprint, Prentice Hall of India, 2000.
4. Douglas a. Pucknell, "Basic VLSI Design" 3rd Edition, Prentice Hall of India, 2000.

UNIT I PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE 9

Statistical distribution , statistical confidence and hypothesis testing ,probability plotting techniques – Weibull, extreme value ,hazard, binomial data; Analysis of load – strength interference , Safety margin and loading roughness on reliability.

UNIT II RELIABILITY PREDICTION, MODELLING AND DESIGN 9

Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis ,petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY 9

Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV RELIABILITY TESTING AND ANALYSIS 9

Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V MANUFACTURE AND RELIABILITY MAQNAGEMENT 9

Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes , reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

TOTAL: 45**REFERENCES:**

1. Patrick D.T. O'Connor, David Newton and Richard Bromley, Practical Reliability Engineering, Fourth edition, John Wiley & Sons, 2002.
2. David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, New York, "AT & T Reliability Manual", 5th Edition, 1998.
3. Gregg K. Hobbs, "Accelerated Reliability Engineering - HALT and HASS", John Wiley & Sons, New York, 2000.
4. Lewis, "Introduction to Reliability Engineering", 2nd Edition, Wiley International 1996.

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS

9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION

9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank order filters.

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS

9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES

9

Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING

9

Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL: 45

REFERENCES:

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation", Wiley, Interscience, 2007.
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004.

UNIT I RANDOM ACCESS MEMORY TECHNOLOGIES**9**

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.

Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures –BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application, Specific DRAMs.

UNIT II NONVOLATILE MEMORIES**9**

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) – Programmable Read-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

UNIT III MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE**9**

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing- Application Specific Memory Testing

UNIT IV RELIABILITY AND RADIATION EFFECTS**9**

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability- Reliability Test Structures-Reliability Screening and Qualification. RAM Fault Modeling, Electrical Testing, Psuedo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

UNIT V PACKAGING TECHNOLOGIES**9**

Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques- Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magnetoresistive. Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

TOTAL: 45**REFERENCES:**

1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ",Prentice-Hall of India Private Limited, New Delhi, 1997.
2. Tegze P.Haraszti, "CMOS Memory Circuits", Kluwer Academic publishers, 2001.
3. Betty Prince, " Emerging Memories: Technologies and Trends", Kluwer Academic publishers, 2002.

UNIT I MECHANICS OF SPEECH**8**

Speech production mechanism – Nature of Speech signal – Discrete time modelling of Speech production – Representation of Speech signals – Classification of Speech sounds – Phones – Phonemes – Phonetic and Phonemic alphabets – Articulatory features. Music production – Auditory perception – Anatomical pathways from the ear to the perception of sound – Peripheral auditory system – Psycho acoustics

UNIT II TIME DOMAIN METHODS FOR SPEECH PROCESSING**8**

Time domain parameters of Speech signal – Methods for extracting the parameters Energy, Average Magnitude – Zero crossing Rate – Silence Discrimination using ZCR and energy – Short Time Auto Correlation Function – Pitch period estimation using Auto Correlation Function

UNIT III FREQUENCY DOMAIN METHOD FOR SPEECH PROCESSING**9**

Short Time Fourier analysis – Filter bank analysis – Formant extraction – Pitch Extraction – Analysis by Synthesis- Analysis synthesis systems- Phase vocoder— Channel Vocoder.

HOMOMORPHIC SPEECH ANALYSIS:

Cepstral analysis of Speech – Formant and Pitch Estimation – Homomorphic Vocoders.

UNIT IV LINEAR PREDICTIVE ANALYSIS OF SPEECH**10**

Formulation of Linear Prediction problem in Time Domain – Basic Principle – Auto correlation method – Covariance method – Solution of LPC equations – Cholesky method – Durbin's Recursive algorithm – lattice formation and solutions – Comparison of different methods – Application of LPC parameters – Pitch detection using LPC parameters – Formant analysis – VELP – CELP.

UNIT V APPLICATION OF SPEECH SIGNAL PROCESSING**10**

Algorithms: Spectral Estimation, dynamic time warping, hidden Markov model – Music analysis – Pitch Detection – Feature analysis for recognition –Automatic Speech Recognition – Feature Extraction for ASR – Deterministic sequence recognition – Statistical Sequence recognition – ASR systems – Speaker identification and verification – Voice response system – Speech Synthesis: Text to speech, voice over IP.

TOTAL: 45**REFERENCES:**

1. Ben Gold and Nelson Morgan, Speech and Audio Signal Processing, John Wiley and Sons Inc. , Singapore, 2004
2. L.R.Rabiner and R.W.Schaffer – Digital Processing of Speech signals – Prentice Hall -1978.
3. Quatieri – Discrete-time Speech Signal Processing – Prentice Hall – 2001.
4. J.L.Flanagan – Speech analysis: Synthesis and Perception – 2nd edition – Berlin – 1972.
5. I.H.Witten – – Principles of Computer Speech – Academic Press – 1982.

UNIT I EMI/EMC CONCEPTS 9

EMI-EMC concepts and definitions, Sources and victim of EMI, Conducted and Radiated EMI, Transient EMI ,Time domain Vs Frequency domain EMI, Units of measurement parameters, ESD, Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES 9

Conducted, radiated and transient coupling, Common impedance ground coupling, Radiated Common mode and ground loop coupling, Differential mode coupling, near field cable to cable coupling, cross talk, Field to cable coupling, Power mains and Power supply Coupling.

UNIT III EMI CONTROL TECHNIQUES 9

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV EMC DESIGN OF PCBs 9

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations, Motherboard Designs and Propagation Delay Performance Models.

UNIT V EMI MEASUREMENTS AND STANDARDS 9

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462. Test beds for ESD and EFT.

TOTAL: 45**REFERENCES:**

1. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, Newyork, 1996.
2. Henry W.Ott., "Noise Reduction Techniques in Electronic Systems", A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
3. Bemhard Keiser, "Principles of Electromagnetic Compatibility", 3rd Ed, Artech house, Norwood, 1986.
4. C.R.Paul, "Introduction to Electromagnetic Compatibility", John Wileyand Sons, Inc, 1992.
5. Don R.J.White Consultant Incorporate, "Handbook of EMI/EMC", Vol I-V, 1988.

UNIT I	WIRELESS MEDIUM AND ACCESS	9
<p>Overview of wireless systems - Air Interface Design – Radio propagation mechanism – Path loss modeling and Signal Coverage – Effect of Multipath and Doppler – Channel Measurement and Modelling – Simulation of Radio Channel. Fixed Assignment Access for Voice Networks – Random Access for Data Networks – Integration of Voice and Data Traffic.</p>		
UNIT II	WIRELESS LAN	9
<p>Introduction to wireless LANs – IEEE 802.11 – WPAN IEEE 802.15 –Mobile AdHoc Networks(MANET)- Principle and operation - Wireless Home Networking – Concepts of Bluetooth Technology – Wireless Geolocation.</p>		
UNIT III	EMBEDDED NETWORK REQUIREMENTS	9
<p>Embedded networking – code requirements – Communication requirements – Introduction to CAN open – CAN open standard – Object directory – Electronic Data Sheets & Device – Configuration files – Service Data Objectives – Network management CAN open messages – Device profile encoder.</p>		
UNIT IV	CAN OPEN	9
<p>CAN open configuration – Evaluating system requirements choosing devices and tools – Configuring single devices – Overall network configuration – Network simulation – Network Commissioning – Advanced features and testing. CAN: Controller Area Network – Underlying Technology CAN Overview – Selecting a CAN Controller – CAN development tools.</p>		
UNIT V	IMPLEMENTATION OF CAN OPEN	9
<p>Implementing CAN open Communication layout and requirements – Comparison of implementation methods – Micro CAN open – CAN open source code – Conformance test – Entire design life cycle. Physical layer – Data types – Object dictionary – Communication object identifiers – Emerging objects – Node states.</p>		

TOTAL: 45

REFERENCES:

1. Glaf P.Feiffer, Andrew Ayre and Christian Keyold, “Embedded networking with CAN and CAN open”, Embedded System Academy 2005.
2. Kaveth Pahlavan, K.Prasanth Krishnamurthy, “Principles of Wireless Networks”, Pearson Education Asia, 2002.
3. William Stallings, “Wireless Communications and Networks”, Second Edition Prentice Hall, India2007.
4. Jon W Mark, Weihua Zhuang, “Wireless communication and Networking”, Prentice Hall India 2003.

UNIT I FUNDAMENTALS OF PROGRAMMABLE DSPs 9

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P-DSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II TMS320C5X PROCESSOR 9

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

UNIT III TMS320C3X PROCESSOR 9

Architecture – Data formats - Addressing modes – Groups of addressing modes-Instruction sets - Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series, Convolution of two sequences, Filter design

UNIT IV ADSP PROCESSORS 9

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation

UNIT V ADVANCED PROCESSORS 9

Architecture of TMS320C54X: Pipe line operation, Code Composer studio - Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

TOTAL: 45**REFERENCES:**

1. B.Venkataramani and M.Bhaskar, “Digital Signal Processors – Architecture, Programming and Applications” – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.
2. User guides Texas Instrumentation, Analog Devices, Motorola.

UNIT I STATISTICAL MODELING 9

Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom's model, Principal component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models

UNIT II STATISTICAL PERFORMANCE, POWER AND YIELD ANALYSIS 9

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation

UNIT III CONVEX OPTIMIZATION 9

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Max- monomial fitting, Posynomial fitting.

UNIT IV GENETIC ALGORITHM 9

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement,routing technology,Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multiway Partitioning Hybrid genetic-encoding-local improvement-WDFR-Comparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.

UNIT V GA ROUTING PROCEDURES AND POWER ESTIMATION 9

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures.Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.

TOTAL: 45**REFERENCES**

1. Ashish Srivastava, Dennis Sylvester, David Blaauw "Statistical Analysis and Optimization for VLSI:Timing and Power" , Springer, 2005.
2. Pinaki Mazumder, E.Mrudnick, "Genetic Algorithm for VLSI Design,Layout and test Automation", Prentice Hall,1998.
3. Stephen Boyd, Lieven Vandenberghe "Convex Optimization", Cambridge University Press, 2004.

UNIT I DIGITAL SYSTEMS**9**

Digital system and VLSI-Transistors-Design rules-Layout design and tools-logic gates-static complementary gates-switch logic-alternative gate circuits-delay through resistive interconnect-delay through inductive interconnect.

UNIT II COMBINATIONAL NETWORK AND SEQUENTIAL NETWORK**9**

Combinational logic network-standard cell based layout- Combinational network delay-logic and interconnect design-power optimization-switch logic network-combinational logic testing. Sequential machines-Latches and Flip-flops-Sequential systems and clocking disciplines-Sequential System Design- Power optimization-Design Validation-Sequential testing

UNIT III SUBSYSTEM DESIGN**9**

Subsystem Design-Principles of Shifters-Adders-ALU-Multiplier-High Density Memory-FPGA-PLA- Floor planning methods- off chip connections-Architectural Design –HDL-Register Transfer Design-High Level Synthesis-Architecture for low power-SoC and embedded CPUs-Architecture testing.

UNIT IV CHIP DESIGN**9**

Chip Design-methodologies-Kitchen Timer Chip-Microprocessor Data Path CAD systems and algorithms-Switch level simulation-layout synthesis-analysis-timing analysis and optimization-logic synthesis-test generation-Sequential machine optimization-scheduling and binding- Hardware/Software co design

UNIT V SOFTWARE AND HARDWARE DESIGN VERIFICATION**9**

Logical verification, Design & Verification languages, Digital simulation, using transactional, level models in an SOC design. Hardware acceleration & emulation, Formal property verification, TEST, DFT, ATPG.

TOTAL: 45**REFERENCES:**

1. Wolf, Wayne "Modern VLSI Design: System-on-Chip Design", 3rd edition, Pearson Edition, New Delhi, 2004.
2. Reis, Ricardo., "Design of System on a Chip: Devices and Components", Springer, 2004.
3. Rashinkar P., Paterson and Singh L., "System on a Chip Verification – Methodologies and Techniques", Kluwer Academic Publishers, 2001.
4. Wang, Laung – Terng, Stroud, Charles.E., Toubia, Nur.A, "System–on–Chip Test Architectures: Nanometer Design for Testability", Elsevier Inc,2007.
5. www.elsevier.com
6. Louis Scheffer Luciano Lavagno and Grant Martin, EDA for IC System verification and Testing, CRC, 2006.

UNIT I BASICS OF TESTING AND FAULT MODELLING 9

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.

UNIT II TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY 9

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS 9

Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS 9

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

TOTAL: 45**REFERENCES:**

1. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House,2002.
2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
3. M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4. A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002.